CADENCE DESIGN CONTEST 2012

SUBMIT AN ABSTRACT TODAY

Deadline: Friday, 13th April, 2012

OPEN TO ALL B.E / B. TECH AND M.E./ M. TECH STUDENTS

The submissions will be judged by an Expert Committee that comprises senior advisors from Cadence's customer base and Cadence experts.

CATEGORIES

There will be two categories for which prizes will be given. A winner will be chosen in both these categories:

- Full time B.E / B. Tech students
- Full time M.E. / M. Tech students

DESIGN REQUIREMENTS

Submissions invited in either Analog, Digital or Board Design in either operational chip design (designs have been implemented and tested) OR Conceptual design (not yet implemented but must have been thoroughly simulated and must include a test plan).

EVALUATION CRITERIA

Submissions are judged by an Expert Committee on the following criteria:

- Inventiveness

• Complexity and feasibility of project

• Breadth of Design

• Effective Use of Cadence technologies

• Presentation and clarity of communication

PRIZE

• Winner in Bachelor's category - Rs. 25,000 per team member to the maximum of Rs. 1 lakh. Guide of winning Bachelor's project - Rs. 35,000.

• Runner up in Bachelor's category - Rs. 20,000 for the team (including guide)

• Winner in Master's category - Rs. 28,000 per team member to a maximum of Rs. 1.12 lakh. Guide of winning Master's project - Rs. 40,000

• Runner up in the Master's category - Rs. 25,000 for the team (including guide)

CONTEST RULES

The University / Institute must be enrolled as part of the Cadence University Program at the time of submitting the abstract for the Contest.

• Maximum of 4 submissions per college

• Maximum of 4 students per submission.

• The design work submission must have taken place as part of the students' course or research work at the university / institute, and must have been completed within 12 months prior to the submission deadline.

• All designs must use predominantly Cadence technology

• Diagrams are allowed.

• Abstract must provide high level specs / framework with measurable parameters that demonstrate the project's uniqueness, such as:

- The intended product / application (specify domains where this will be valuable)

- Enhanced low power consumption (capability to turn off battery power for longer)

- Increased performance (increase of throughput and time saving achieved)

- Newer functionality introduced

- Verifications frameworks used

• Abstract must clearly describe how Cadence tools helped in the design analysis, decisions and debugging

• Abstract must quantify the completeness of the implementation Vs. original specifications of the project/ design work. Gaps in implementation must be identified and their impact to the original intent of the project/ design work must be evaluated

SAMPLE PROJECT TITLES FROM PREVIOUS DESIGN CONTESTS

Bachelor's category:

• Design and Analog VLSI Implementation of Neural Architecture

• Design and Implementation of a High Speed Power Efficient Hybrid Mode Sense Amplifier for SRAM Applications

• Implementation of a Low Power, Area Efficient Health Analyzer, HealthComm

Master's category:

• Novel High-Performance ROM-less DDFS for Software Defined radio

• A 2.4 GHz Ultra Low Power, Ultra Low Voltage Low Noise Amplifier Design

• Scalable Constant Resistance, Transconductance, GM/C and their Applications

HOW TO SUBMIT

• Register online at **www.cadence.com/in** Download the Abstract Submission Form at the end of the registration process.

• You MUST submit the filled in Abstract Submission Form as the first page of the abstract.

• Email your abstract in Word format ONLY to **designcontest_india@cadence.com**

TIMELINE

Call for papers open	Monday, 20th Feb 2012
Call for papers closed	Friday, 13th April 2012

Submitters informed - 1st round	Friday, 8th June 2012
Papers due from submitters - 2nd round	Friday, 20th July 2012
Submitters informed - 2nd round	Tuesday, 28th Aug 2012
Top teams final live presentation	September 2012
Winners announced	September 2012